REMARKS

Reconsideration of the application is respectfully requested. Pursuant to the agreement reached during the January 8, 2004 telephonic interview with the Examiner, applicant hereby elects, without traverse, Group 1 consisting of claims 1-20. Accordingly, applicant hereby cancels Group 2 consisting of claims 21-24. The substance of the January 8, 2004 telephonic interview is summarized in the Interview Summary form prepared, signed, and dated January 13, 2004 by the Examiner. The Interview Summary is hereby incorporated by reference. Applicant intends to pursue the prosecution of the cancelled claims 21-24 by way of a later divisional application. Claims 1, 4, 5, 13, 14, 15, 17, and 20 have been amended.

Claim Objections

Applicant has amended claim 5 as suggested by the Examiner, i.e., to read ". . . said differential vector data set attached with header forms . . . ."

Applicant has amended claim 14 as suggested by the Examiner. Specifically, in line 5, the comma (",") after the word "set" has been omitted.

The Office Action objected to claim 15 because the "term 'program' in 'A program storage device...' is not clear." The Office Action further noted that claim 15 should read "A programmable storage device . . . ." Applicant respectfully traverses the Examiner's objection on this ground, as the specification makes clear that "a program storage device" is a device that has the capability to store a program that creates redundant vectors. Specifically, for example, the specification on page 10, lines 24-26 discloses that "[r]edundant vectors . . . could be created by a software algorithm; for example, software which interfaced with ATPG software executed on a computer system upstream from the tester." The specification thus makes clear what a

"program storage device" covers, for example, a computer system that executes an ATPG software.

Applicant also respectfully traverses the Examiner's objection that in line 3, "a" needs to be inserted before "original test vector data", because the word "data" includes the plural.

Applicant has amended claim 17 to read "A method for reducing test data volume in the testing of logic products comprising: . . ."

The above amendments are supported throughout the specification. No new matter has been added. Applicant respectfully submits that claim objections have been overcome.

Rejections Under 35 U.S.C. § 112

The Office Action has rejected claim 1 because "[t]he term 'highly' in lines 4 and 6 of claim 1 and throughout various claims is not a positive limitation." In response, Applicant has omitted the term "highly" from claims 1, 5 and 13. Applicant therefore respectfully submits that claims 1, 5, and 13 are allowable.

The Office Action has rejected claim 4 because "[t]he term 'approximately' in line 2 is a relative term and cannot be given patentable weight." In response, Applicant has amended claim 4 to read: "The method of claim 3, wherein said XORing sets ~~approximately half~~ more than a predetermined portion of said care bits to a value of 0 in said differential vector data set~~.~~, wherein said predetermined portion of said care bits can exceed half of said care bits." This amendment is supported throughout the specification, with particular reference to page 6, lines 24-26 and page 7, lines 1-5. No new matter has been added. Applicant therefore respectfully submits that claim 4 is allowable.

The Office Action has rejected claim 13 because there is insufficient antecedent basis for the limitation ". . . said instructions . . . ." Applicant, as suggested by the Examiner, has amended claim 14 to read ". . . said computer-executable instructions . . . ." Applicant therefore respectfully submits that claim 14 is allowable.

The Office Action has rejected claim 15 because "[t]he term 'tangibly' in line 1 is a relative term and cannot be given patentable weight." In response, as suggested by the Examiner, Applicant has omitted the term "tangibly." The Office Action has further rejected claim 15 as being not clear because there allegedly is no first test vector in the original test vector data. Applicant respectfully traverses the Examiner's rejection on this ground, as the specification makes clear that an original test vector data can be divided into different subsets of test vector data. Specifically, on page 10, lines 5-19 of the specification, in conjunction with Figs. 6A and 6B, an example is disclosed where the original test vector data is divided into different subsets of test vector data and numbered accordingly. Applicant therefore respectfully submits that claim 15 is allowable.

The Office Action has rejected claim 20 because "[t]he term 'approximately' in line 2 is a relative term and cannot be given patentable weight." In response, Applicant has amended claim 20 to read: "The method of claim 19, wherein said XORing sets ~~approximately half~~ more than a predetermined portion of said care bits to a value of 0~~.~~, wherein said predetermined portion of said care bits can exceed half of said care bits." This amendment is supported throughout the specification, with particular reference to page 6, lines 24-26 and page 7, lines 1-5. No new matter has been added. Applicant therefore respectfully submits that claim 20 is allowable.

Rejections Under 35 U.S.C. § 103

The Office Action has rejected claims 1-20 under 35 U.S.C. § 103 as being unpatentable over Rajski et al. U.S. Patent 6,327,687 (hereinafter "Rajski") further in view of Rohrbaugh et al. U.S. Patent 6,067,651 (hereinafter "Rohbaugh"). Applicant respectfully traverses this rejetion.

The Office Action incorrectly states that Rajski in combination with Rohrbaugh renders claims 1, 9, 13, 15, and 17 obvious. As noted by the Examiner, Rajski does not explicitly teach filling don't-care bits of the original test vector data with repeated values. Nor does Rajski implicitly teach such limitation. Rather, Rajski teaches away from filling don't-care bits of the original vectors with repeated values: "The remaining scan cells in the test cube may be left unassigned and are filled with a **pseudo-random test pattern** generated by the decompressor during testing. Thus, the ATPG tool generates test vectors without filling in the 'don't care' positions with random patterns." (Rajski at 5:3-7) (emphasis added). As such, the present invention differ at least in two aspects from Rajski: First, in the present invention, as noted by the Examiner, don't care bits are filled with repeated values, whereas in Rajski, don't care bits are filled with pseudo-random values. A pseudo-random value by definition has an opposite meaning to a repeated value. (*See e.g.*, Webster's New World College Dictionary (4th ed. 1999), at p.1187 (defining "random" as "not uniform.")). Second, in the present invention, don't-care bits of the original test vector data are filled with repeated values **before** the test vectors are compressed and used for testing a logic product. (*See e.g.*, page 4, line 10 – page 5, line 10 of the present specification). In contrast, in Rajski, don't care bits are filled in with pseudo-random patterns "by the decompressor **during** testing." (Rajski at 5:5-6) (emphasis added).

The Office Action also incorrectly states that "Rohrbaugh teaches setting the don't cares to a repeated value." (Office Action at page 8, line 8-9). Rohrbaugh in fact plainly and

explicitly teaches to the contrary: "[T]he don't care bit positions of the substantially compacted vector are **random filled** (with 1s and 0s) and fault is simulated and a new test vector is generated." (Rohrbaugh at 3:15-18) (emphasis added). In fact, the crux of Rohrbaugh's method for compacting is eliminating redundant test vectors by **randomly** filling don't care bits:

> Specifically, arbitrary filling may be utilized to eliminate redundant vectors in the set. For example, don't care values of the first vector in the set may be random filled. This vector may then be again evaluated to determine whether it detects any additional faults, **as a result of the random filled values**.

(Rohrbaugh at 10:49-54) (emphasis added). Thus, if don't care bits of the substantially compacted test vectors are filled with repeated values as suggested by the Examiner, the above advantage as a result of random filling will simply vanish. Moreover, Rohrbaugh explicitly teaches that don't care bit positions of the substantially **compacted** vector are random filled, whereas in the present invention, the non-care bit positions of the **original** test vectors (i.e., pre-compaction test vectors) are filled with repeated values. (*See e.g.*, Specification at page 4, line2-15).

As shown, because neither Rajski nor Rohrbaugh teaches filling don't care bits in original test vectors with repeated values, it would have not been obvious to one of ordinary skill in the art at the time the present invention was made to modify Rajski by utilizing Rohrbaugh to achieve the teachings of the present invention. Applicant thus respectfully submits that claims 1, 9, 13, 15, and 17 are patentable over Rajski and Rohrbaugh.

Applicant respectfully submits that claim 2 is allowable over Rajski and Rohrbaugh because it is dependent on claim 1, an allowable claim as discussed previously.

The Office Action incorrectly equates the background vector data set of claims 3 and 8 of the present invention with the test cube of Rajski. A test cube is "a deterministic pattern of bits

wherein each bit corresponds to a scan cell in the scan chains. Some of the scan cells are assigned values (e.g., a logic 1 or logic 0), while other scan cells are 'don't cares.'" (Rajski at 8:50-57). To the background vector of the present invention, however, care bits (i.e., "assigned values") and/or don't care bits have no meaning. Rather, "[t]he background vectors may be all 0s, all 1s, or a random distribution of 0s and 1s[,]" because the background vectors are utilized to set don't care bits of the original test vectors with repeated values. (Specification at page 5, lines 1-8). Furthermore, nowhere in Rajski even suggests the concept of "background vectors" as disclosed in the present invention.

The Office Action also improperly states that Rajski in Figure 7 teaches forming a differential vector data set by XORing care bits with background vector bits. Initially, as explained above, there are no "background vector bits" or their equivalents in Rajski that can be XORed with care bits of an original test vector. Moreover, the XOR function in Rajski serves a different purpose than that of the present invention. Specifically, the XOR function in Rajski is concerned with shifting the phase of inputs from the linear finite state machine 46. (*See* Rajski at 7:63-8:20; Figs. 3 & 4). In contrast, the XOR function in the present invention is conducted to generate repetitive patterns in differential vector data sets. (*See* Specification at page 5, lines 5-10).

The Office Action incorrectly states that "Rajski teaches XORing sets a substantial portion of the care bits to a value 0 in Table 8 (column 13, lines 44-59)." Initially, Rajski plainly provides that the equations in Table 8 are applied to Table 7 to generate Table 8. The equations in Table 8, however, do not affect the cares bits of Table 7 as shown in Table 9, wherein the care bits, which are underlined, have the same value as the care bits in Table 7. Moreover, the

equations in Table 8 do not set even the don't cares in Table 7 to repetitive values. (*See* Rajski at Table 9).

The Office Action incorrectly states that Rajski "teaches an algorithm (Gauss-Jordan elimination) used in header identification and a seed used to generate vector data . . . ." As also suggested in Rajski, the well-known Gauss-Jordan elimination technique is used to solve a system of linear equations. (*See* Rajski at 10:62-66). The algorithm referred to in claim 5 of the present invention has nothing to do with solving linear equations; rather, a given algorithm is used to generate a set of background vectors specific to that algorithm. (*See* Specification at page 6, lines 6-9). Moreover, nowhere in Rajski discloses or even suggests a data set header is attached to any differential vector, which, as explained above, is also a non-existent concept in Rajski.

The Office Action incorrectly states that Rajski teaches the step recited in claim 6 of the present invention. As shown above, Rajski is devoid of any concepts of differential vectors, background vector data set, or header as disclosed in the present invention. Similarly, claim 7 of the present invention, which is dependent on claim 6, is not taught by Rajski.

The Office Action incorrectly states that Rajski teaches "a random distribution of bits having both '0' and '1' in column 3, lines 10-11 . . . ." "Weighted random patterns," as suggested in Rajski, themselves are "test patterns," that is, a set of data that are fed, unaltered in their form, into a logic device under test. (*See* Rajski at 2:34-40). In contrast, the background vector data set of the present invention is not a "test pattern." The original test vector of the present invention is the "test pattern," and it is XORed with the background vector to generate the differential vector. (*See* Specification at page 5, lines 5-10). One of the reasons that the background vector of the present invention is chosen to have random fill patterns is to enhance

the probability of generating more repeated values in a differential vector. (*See* Specification at page 5, lines 24-26 – page 6, lines 1-5). This is in contrast to "weighted random patterns" where random fill pattern is utilized to uncover hard-to-test faults. (Rajski at 2:32-67 – 3:18).

The Office Action incorrectly states that "Rajski et al. teaches a different care bit is repeated in the same column for each row of the matrix in Table 4 (column 11, lines 24-34)." If this were true, than, for example, the only care bit of "1" in column 8 (the far-right column) of Table 2 should have been repeated in rows 0 to 7. However, as shown in Table 4, column 8 in Table 4 has "0"s and "1"s.

Applicant respectfully submits that claim 14, which is dependent on claim 13 that is allowable as shown above, is also allowable over Rajski and Rohrbaugh.

Based on the foregoing, Applicant respectfully submits that this application is in condition for allowance, which is respectfully requested.

Should the Examiner have any questions or comments on the application, the Examiner should feel free to contact the undersigned via telephone.

Respectfully submitted,

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